Graphene Flash Memory

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ABSTRACT Graphene's single atomic layer of sp^2 carbon has recently garnered much attention for its potential use in electronic applications. Here, we report a memory application for graphene, which we call graphene flash memory (GFM). GFM has the potential to exceed the performance of current flash memory technology by utilizing the intrinsic properties of graphene, such as high density of states, high work function, and low dimensionality. To this end, we have grown large-area graphene sheets by chemical vapor deposition and integrated them into a floating gate structure. GFM displays a wide memory window of ~6 V at significantly low program/erase voltages of ±7 V. GFM also shows a long retention time of more than 10 years at room temperature. Additionally, simulations suggest that GFM suffers very little from cell-to-cell interference, potentially enabling scaling down far beyond current state-of-the-art flash memory devices.

KEYWORDS: graphene · nonvolatile flash memory · memory window · retention time · cell-to-cell interference

Graphene has emerged as a fascinating platform because its planar atomic structure and high symmetry lead to a variety of superlative electronic and physical properties. Most recent achievements fall broadly into one of two categories: first, those that elucidate or exploit the intrinsic in-plane characteristics of graphene (*e.g.*, field-effect transistors [FETs][1,2] and high tensile strength films[3,4]), and second, those that utilize the material's single atomic profile as the low-thickness limit of some scalable thin-film systems such as ultracapacitors[5,6] or transparent conductors.[7,8] Here we show that graphene is an excellent platform for flash memory, one that may indeed help overcome several challenges faced by current industry standards.[9,10]

To date, graphene has been incorporated into several types of nonvolatile memory structures, where each memory type operates on a unique physical mechanism. For example, Echtermeyer *et al.*[11] show bistable state operation through chemical modification of graphene to form insulating graphene derivatives in graphene FETs, while Standley *et al.*[12] and Son *et al.*[13] utilize the filament effect to produce memory functionality in a two-terminal resistor structure. Nano/micro-electromechanical switches (NEMS/MEMS) exploiting graphene's low mass density and high Young's modulus have also been realized by Milaninia *et al.*[14] and Kim *et al.*,[15] which show promise for low power memory applications. Furthermore, the hysteresis effect in graphene ferroelectric-field-effect transistors (FFETs) comprised of a ferroelectric gate oxide and a graphene channel has proven to be an alternative to conventional semiconducting FFETs.[16−18]

All of the aforementioned memory types are currently being considered as emerging technologies for nonvolatile memory applications because of the limitations encountered in flash technology when attempting to increase storage capacity by miniaturization. In order to recognize the bottleneck of conventional flash technology, we must first understand the structures and operating mechanisms of flash memory. There are two types of flash memory structures: floating-gate flash memory (FG), which is the current industry standard, and charge-trap flash memory (CT), which is an emerging technology. Flash memory, in general, is comprised of a p-type silicon channel substrate, a tunnel oxide, a semiconducting highly doped n-type polysilicon (FG) or an insulating silicon nitride (CT) data storage layer, a control oxide, and a gate electrode. Writing is achieved by applying a voltage pulse on the gate electrode, which allows electrons to tunnel through the tunnel oxide from the silicon channel to the storage layer. This causes a positive shift in the threshold voltage (V_{th}) of the memory device and is simply the additional voltage required to compensate the stored charges in the storage layer. The binary values are defined by the current upon a read

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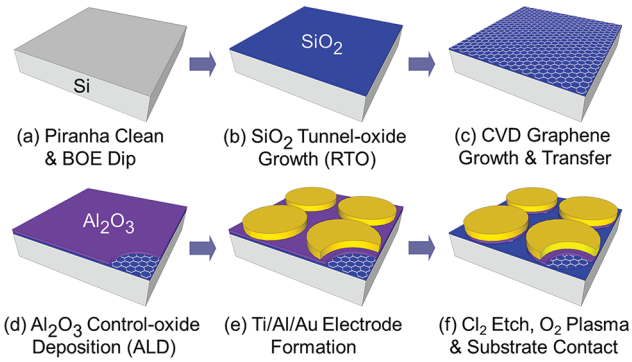

Figure 1. GFM fabrication processes. (a) Piranha rinsing and BOE dip of Si substrate. (b) Tunnel oxide (SiO_2) formation through RTO. (c) CVD graphene growth and transfer. (d) Control oxide (Al_2O_3) deposition by ALD. (e) Gate-electrode (Ti/Al/Au) formation using standard photolithography technique. (f) Device isolation by Cl_2 dry etching (Al_2O_3) and O_2 plasma. Finally, substrate contact (Pt) by e-beam evaporation.

cycle at a voltage within the width of the threshold voltage shift.

The primary goal of most research in flash memory is to increase the density of storage elements such that their parent devices can be miniaturized, which leads to confronting several challenges that would normally jeopardize device performance at the reduced scale. As the device dimensions become smaller (<30 nm), FG suffers from a lower gate-coupling ratio (GCR, the ratio of the voltage drop across the tunnel oxide and the total voltage across the channel and gate, *i.e.*, the amount of capacitive coupling from the gate to channel) and increasing crosstalk between neighboring floating gates.[10] CT, on the other hand, has a single gate to control the channel directly, which allows a high GCR, and an insulating nitride storage layer, which has insignificant interference. Upon scaling, however, CT can become hindered through variability in V_{th} caused by the implementation limit of trap density ($\sim 10^{19}$ cm^{-3}) and uniformity,[10] and short retention times due to shallow trap energy levels that can promote trap-assisted Poole–Frenkel conduction during the retention state.[19]

Graphene has the potential to exceed the performance of current flash memory technology by utilizing the exceptional intrinsic properties of graphene, such as high density of states, high work function, and low dimensionality when compared to the conventional FG and CT materials. Recently, it was shown that incorporation of an insulating form of graphene, known as graphene oxide, acts as an effective charge storing layer in CT devices.[20] In its natural semimetallic form, graphene can act as the floating gate in FG devices. Although memory devices can be characterized along a wide variety of metrics, in this study, we specifically address the benefits of metallic graphene in a FG structure with an eye toward the width of the memory window, retention time, and cell-to-cell crosstalk at low operating voltages.

RESULTS AND DISCUSSION

In order to investigate the electrical characteristics of graphene flash memory (GFM), a number of devices were fabricated with the following process flow as shown in Figure 1. First, a 4 in. boron-doped ($\sim 10^{15}$ cm^{-3}) Si wafer was cleaned sequentially by a Piranha solution ($H_2SO_4 + H_2O_2$) and then dipped into a buffered oxide etchant (BOE, $HF + NH_4F + H_2O$) to remove any residual native oxide (Figure 1a). Second, a SiO_2 tunnel oxide of 5 ± 0.2 nm was grown for 7 s through rapid thermal oxidation (RTO) at 1000 °C, under an oxygen flow of 40 sccm (Figure 1b). After the graphene sheets were transferred (see Materials and Methods) onto the tunnel oxide surface (Figure 1c), Raman spectroscopy was used to ensure the quality of the transferred single layered graphene (SLG) and multilayered graphene (MLG) (Figure 2e and f).[21] Third, a control oxide of 35 ± 1 nm was formed by evaporating a 1.1 nm thick Al layer, oxidizing in air for 2 days, and depositing 300 cycles of additional Al_2O_3 through atomic layer deposition (ALD) (Figure 1d).[22] Gate electrodes of Ti/Al/Au (10 nm/500 nm/50 nm) with various areas (2.5×10^{-5} to 7×10^{-4} cm^2) were defined and deposited using photolithography and an e-beam evaporator (Figure 1e). In order to isolate each memory device, the Ti/Al/Au gate electrodes were used as a mask to etch the gate stacks. The Al_2O_3 layer and graphene present outside the device area were removed with a 30 s Cl_2 reactive ion etching (UNAXIS SLR770), followed by 3 min of O_2 plasma. Finally, a 50 nm thick Pt back contact was made by e-beam evaporation (Figure 1f). Figure 2a–d show transmission electron micrograph (TEM) cross sections of both as-fabricated single-layer and multilayer GFM devices.

An important figure of merit for flash memory is the memory window, which refers to the shift in threshold voltage of the memory device when switching from the 0 to 1 binary states. Industry standards suggest that a minimum width of 1.5 V is necessary to produce a reasonable on/off ratio for reliable memory functionality. For standard FG devices using polysilicon, this requires a program/erase voltage of around ±20 V.[10] This large voltage requirement is due to the low density of states (DOS) in the degenerately doped polysilicon, which leads to the necessity of high GCRs.

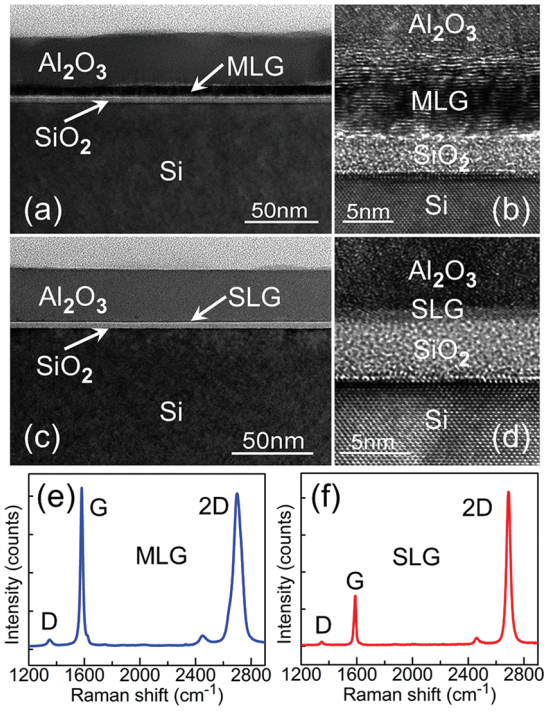

Figure 2. Cross-sectional TEM images of GFM. (a) TEM image of MLGFM with 35 ± 1 nm Al_2O_3 control oxide grown on MLG. (b) HR-TEM image of MLGFM showing graphene layers and the 5 ± 0.2 nm SiO_2 tunnel oxide. (c) TEM image of SLGFM. (d) HR-TEM image of SLGFM. (e) Raman spectrum of MLG on tunnel oxide. (f) Raman spectrum of SLG on tunnel oxide.

In contrast, graphene offers a semimetallic band structure, with a high DOS away from the Dirac point. The same can be said for any metal, which begs the question of why metals are not implemented as charge-storage layers. The answer lies in the fact that high migration of metal atoms renders them unsuitable for many device applications compared to graphene's inert covalently bonded honeycomb structure. Graphene's higher DOS lowers the field required for programming, which permits a greater range of engineering solutions. For example, one can think of planar device structures, which produce lower GCRs, but may still be sufficient given the lower field requirement.

Figure 3 shows the electrical characteristics of as-fabricated devices along with a control, which is fabricated under identical procedures without the addition of graphene layers. While the SLG devices (Figure 3b) exhibit a window width of ~2 V using a program/erase voltage of ±7 V, MLG devices (Figure 3a) show a window width of ~6 V. The greater memory window of the MLG devices is directly attributable to a larger thickness present in MLG as compared to that in SLG. The smaller memory window in the SLG flash memory (FM) compared to the MLG-FM is a result of the SLG being only one atom thick (~0.35 nm), which is thinner than the interlayer screening length of the MLG (λ = 0.6–1.2 nm).[23–25] In a conductive medium, the stored charges redistribute

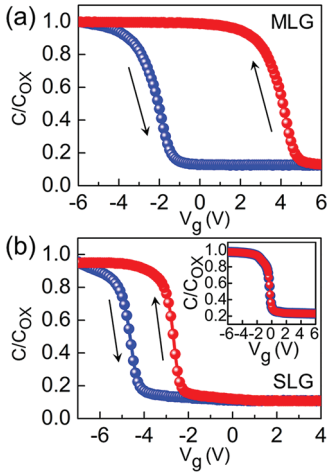

Figure 3. Capacitance–voltage (*C*–*V*) measurements on GFM and a control sample without graphene. (a) MLG flash memory exhibits counterclockwise hysteresis with a 6 V memory window using a program/erase voltage of ±7 V. (b) SLG flash memory shows a 2 V memory window at a negative threshold voltage due to hole doping in graphene. Inset: *C*–*V* characteristics of the control device show negligible hysteresis. All capacitance values were normalized with respect to the capacitance of the control oxide (C_{ox}).

themselves on the surface to minimize the coulomb potential energy. The characteristic thickness in which the charges reside is called the Thomas–Fermi (T-F) screening length. In general, metals have an extremely short T-F screening length of only several atomic layers, whereas the one atom thick graphene stores charge in a single layer. By adopting a theoretical model[24] and using the ratio of the stored charges (memory window) between our MLG-FM and SLG-FM, $N_{MLGFM}/N_{SLGFM} \approx 1.0 \times 10^{13}\ cm^{-2}/3.33 \times 10^{12}\ cm^{-2} \approx 3$ ($\approx \Delta V_{MLGFM}/\Delta V_{SLGFM} \approx$ 6 V/2 V ≈ 3), we find the screening length to be λ = 0.8 nm, which is consistent with reported values.[23–25] Given the insignificant memory (~20 mV) observed in the control device (inset of Figure 3b) and a small unintentional hysteresis induced by interface traps (~10^{10}–10^{11} cm^{-2}) in graphene/SiO_2 FETs,[26] we conclude that the charges responsible for the wide memory window are stored in the graphene layer(s).

The counterclockwise memory effects, as indicated by arrows in each plot in Figure 3a and b, show that electron transfer through the tunnel oxide dominates the electron charge–discharge rate. Conversely, a clockwise memory effect can arise due to a leaky control oxide, resulting in electron transfer through the control oxide,[27] and thus cannot be used in integrated circuits. A minimal leakage current of 7 × 10^{-7} A/cm^2 at a gate voltage (V_g) of −10 V corroborates charge transfer through the tunnel oxide (see Supporting Information).

We noticed that the initial threshold voltage (forward bias regime) of the SLG-FM shows a large negative value (−3.89 V) compared to the threshold voltage of the MLG-FM (−1.33 V). This large negative

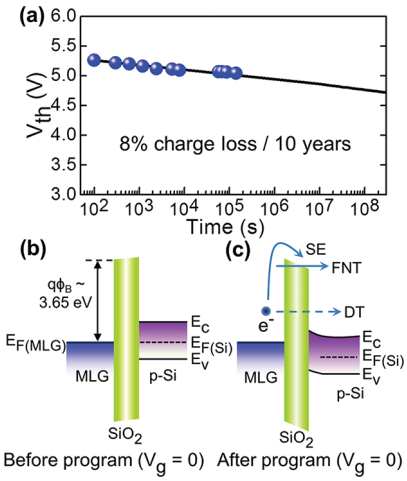

Figure 4. Retention characteristics of GFM. (a) Retention measurement of MLG-FM showing only 8% of charge loss in 10 years at room temperature. (b) Energy band diagram of MLG/SiO_2/Si junctions before programming. (a) Energy band diagram after programming, which shows three possible mechanisms for charge loss during retention state: SE, FNT, and DT. All three mechanisms depend exponentially on the barrier height (ϕ_B) between the work function of graphene and the SiO_2 tunnel oxide.

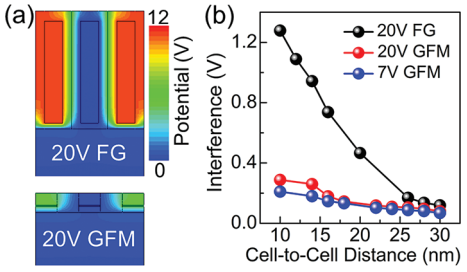

Figure 5. Cell-to-cell crosstalk in polysilicon FG flash memory and GFM. (a) Simulated potential profiles with three flash memory cells in series for FG and GFM at a program voltage of 20 V. (b) Comparison of interference depending on cell-to-cell distance between FG and GFM. Interference is defined as the shift of V_{th} of the unprogrammed cell (middle) influenced by the two nearest neighbor cells. Simulation results show significant interference that can cause a bit error in FG because of the large side-wall capacitance. In contrast, the thinness of graphene lowers the crosstalk and makes it desirable for miniaturization.

threshold voltage in the SLG-FM is observed as we need to apply an additional electric field to compensate for the holes and invert the p-type Si substrate. This indicates that SLG is inherently p-type, which is consistent with reports that graphene is doped by atmospheric molecules, photoresist residue, metal etchants, and Al_2O_3.[22,28−30] Additionally, interface states at the oxide/graphene interface created by defects in graphene (the D band in Raman spectra)[21,31] or dangling bonds of the oxide can induce additional positive charges inside the gate stack. All of the above can be applied to both SLG and MLG. However, MLG will be less sensitive to charge doping effects since the additional layers will screen and lessen the effects of these charges. Accurate contributions from defects and doping to initial threshold voltages should be further investigated.

The next figure of merit for flash memory devices is retention time, which refers to the potential lifetime of nonvolatile storage. Generally, retention time requirements are more than 10 years before the device loses 50% of stored charge.[10] Loss of storage is typically the result of charge tunneling from the floating gate through the tunnel oxide. The rate of tunneling is dependent on the height and thickness of the electronic barrier presented by the tunnel oxide. In traditional polysilicon/SiO_2 FG devices, the barrier height is fixed and simply the difference between the SiO_2 conduction band edge (0.95 eV) and that of polysilicon (4.02 eV), which implies that the minimum tunnel oxide thickness is limited to 7−8 nm. In contrast, the graphene/SiO_2 system offers a larger electronic barrier height due to the higher work function of graphene (~4.6 ± 0.05 V near the Dirac point),[32] which allows the tunnel oxide to be further thinned.

Figure 4 shows the energy band diagram of our MLG/SiO_2/Si junction and experimental data for retention time of MLG-FM at room temperature with a SiO_2 tunnel oxide of only 5 ± 0.2 nm (*i.e.*, a 30−40% thinner tunnel oxide than that used for polysilicon devices). Measurements indicate that a charge loss of only 8% should occur after 10 years, which is more than adequate for practical devices (Figure 4a). In order to understand the long retention time, multiple charge loss mechanisms can be considered; Schottky emission (SE), Fowler−Nordheim tunneling (FNT), Poole−Frenkel tunneling (PFT), and direct tunneling (DT). Under a normal retention state ($V_g = 0$) the electronic structure at the device interface is different before and after programming, which is illustrated in the band diagrams of Figure 4b and c. This is a result of the creation of an internal field across the tunnel oxide by stored charges in MLG ($N_{MLGFM} \approx 10^{13}$ cm^{-2}). Both the existence of the large barrier height (~3.65 eV) and low electric-field across the tunnel oxide make DT the most likely candidate for charge loss since the other mechanisms require high electric fields to contribute significantly.[33] However, DT is a low-probability event. Thus, we believe that the DT mechanism is attributable to the long retention time of the constructed GFM devices.

The final figure of merit that we examine for flash memory is cell-to-cell interference. For a 2D planar configuration, a given storage element is mainly influenced by its two nearest neighbors, which share the same word line to their gates. This leads to variability in V_{th}, and accordingly, a bit error can easily occur between nearest neighbors when interference is significant. This is a complex interplay because the increasing thickness of the charge storage layer increases the GCR and hence lowers the operating voltage, but also

increases the interference mainly due to an increase in side-wall capacitance. A careful optimization must take place in order to minimize both the operating voltage and cell-to-cell interference. Graphene offers a unique solution to this problem due to its thinness, which minimizes the resulting field upon charging by nearest neighbors and, hence, lowers the crosstalk between nearest neighbors. In some sense, lower interference is a result of graphene's lower GCR.

Simulations of both traditional polysilicon/SiO_2 and thin film metal-based devices are presented in Figure 5. The simulation is based on a thin film metal of 1 nm (~ trilayer graphene), which is the T-F screening length of MLG with a work function of graphene corresponding to 4.6 eV. The simulation results provide an upper limit for graphene devices, since graphene's DOS is less than conventional metallic systems. To understand the maximum interference in a given cell, we simulate the situation where two nearest neighbors are programmed at high gate voltages, while a given cell remains unprogrammed. We then monitor the V_{th} shift of the unprogrammed cell due to its nearest neighbors. Simulation results show that the conventional FG experiences abruptly increasing interference as the device is scaled down below the 25 nm node. However, our GFM shows negligible interference down to a 10 nm cell-to-cell distance. The weakening of this interference effect shows that graphene displays an advantage over polysilicon for this application.

On the basis of our device performance, we can roughly estimate the power reduction and increase in storage density compared to conventional FG. GFM requires half the operating voltage to achieve a 1.5 V memory window, which potentially reduces the operation energy per bit by ~75%, assuming the capacitive charging energy is the limiting factor of such a device. Furthermore, the reduction of cell-to-cell crosstalk shows potential for twice the charge storage density at current industry standards of 0.2 V cell-to-cell interference.[34]

CONCLUSIONS

In summary, our experiments demonstrate the benefits of graphene as a platform for flash memory. The high density of states, high work function, and low dimensionality positively influence device performance, leading to a wide window of operation at low voltages, long retention time, and low cell-to-cell interference. The simulations pertaining to cell-to-cell interference further suggest that graphene may be instrumental in the next round of miniaturization of flash memory.

MATERIALS AND METHODS

Graphene Growth and Transfer. SLG (or MLG) was grown on 25 μm thick Cu foils (or 400 nm thick Ni films deposited onto SiO_2 substrates) by CVD using a tube furnace at 1000 °C (or 950 °C) for 15 min (or 3 min) under flowing precursors of CH_4:H_2 = 100:25 sccm (or 50 or 250 sccm) at a growth pressure of 6 Torr (or 10 Torr). Prior to the growth, samples were annealed at 1000 °C for 30 min under H_2 to remove oxide and enlarge catalyst grains. After the growth, cooling was performed at a rate of approximately 20 °C/min under conditions identical with the growth.[35]

In order to transfer the graphene sheets onto the tunnel oxide, polymethylmethacrylate (PMMA) was spin-coated onto the resulting graphene-coated Cu foils (or Ni films) to protect the graphene sheets and act as a rigid support after the Cu (or Ni) was etched away in an aqueous bath of $FeCl_3$/HCl (or diluted HCl). After the transfer was complete, PMMA was removed in acetone.[36]

Electrical Measurements. All $C-V$ measurements were carried out using a Keithley CV 590 at f = 100 kHz with ramping rate (1 V/s), voltage step (0.1 V), and step interval (100 ms).

Simulations. The simulation on potential distribution and cell-to-cell interference was obtained through Sentaurus (Version D-2010.03) from Synopsys. A 1 nm thick conductor (~trilayer graphene) with a work function of 4.6 eV was used to simulate graphene. The device dimensions and materials were identical on both devices except for the charge-storage layers. The parameters used in the simulation were a 5 nm SiO_2 tunnel oxide, a 10 nm SiO_2 control oxide, 10^{17} cm^{-3} silicon substrate doping, 10^{20} cm^{-3} source/drain doping, and a SiO_2 insulation material between adjacent cells. For cell-to-cell interference, the floating-gate material and the insulation material present between adjacent cells are the dominant factors in FG structure. The use of a 10 nm SiO_2 control oxide instead of 35 nm Al_2O_3 does not substantially affect the interference between cells nor diminish the capacitive coupling on the channel. A high substrate doping and the maximum transconductance (g_m) method were used to circumvent short channel effects, particularly drain-induced barrier lowering, and determine the V_{th}, respectively.

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Supporting Information Available: This section includes the calculation method for stored charge density, the extraction method for V_{th}, measurements of the leakage current, and a simulated interference electric-field profile of GFM. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
2. Liao, L.; Lin, Y.-C.; Bao, M.; Cheng, R.; Bai, J.; Liu, Y.; Qu, Y.; Wang, K. L.; Huang, Y.; Duan, X. High-Speed Graphene Transistors with a Self-Aligned Nanowire Gate. *Nature* **2010**, *467*, 305–308.
3. Bunch, J. S.; van der Zande, A. M.; Verbridge, S. S.; Frank, I. W.; Tanenbaum, D. M.; Parpia, J. M.; Craighead, H. G.; McEuen, P. L. Electromechanical Resonators from Graphene Sheets. *Science* **2007**, *315*, 490–493.
4. Lee, C.; Wei, X.; Kysar, J. W.; Hone, J. Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene. *Science* **2008**, *321*, 385–388.

5. Stoller, M. D.; Park, S.; Zhu, Y.; An, J.; Ruoff, R. S. Graphene-Based Ultracapacitors. *Nano Lett.* **2008**, *8*, 3498–3502.
6. Liu, C.; Yu, Z.; Neff, D.; Zhamu, A.; Jang, B. Z. Graphene-Based Supercapacitor with an Ultrahigh Energy Density. *Nano Lett.* **2010**, *10*, 4863–4868.
7. Nair, R. R.; Blake, P.; Grigorenko, A. N.; Novoselov, K. S.; Booth, T. J.; Stauber, T.; Peres, N. M. R.; Geim, A. K. Fine Structure Constant Defines Visual Transparency of Graphene. *Science* **2008**, *320*, 1308.
8. Bae, S.; Kim, H.; Lee, Y.; Xu, X.; Park, J.-S.; Zheng, Y.; Balakrishnan, J.; Lei, T.; Ri Kim, H.; Song, Y. I.; *et al*. Roll-to-Roll Production of 30-in. Graphene Films for Transparent Electrodes. *Nat. Nano* **2010**, *5*, 574–578.
9. Lu, C.-Y.; Hsieh, K.-Y.; Liu, R. Future Challenges of Flash Memory Technologies. *Microelectron. Eng.* **2009**, *86*, 283–286.
10. International Technology Roadmap for Semiconductors. *ITRS reports* [Online], 2009−2010 (www.itrs.net/reports.html).
11. Echtermeyer, T. J.; Lemme, M. C.; Baus, M.; Szafranek, B. N.; Geim, A. K.; Kurz, H. Nonvolatile Switching in Graphene Field-Effect Devices. *IEEE Electron Device Lett.* **2008**, *29*, 952–954.
12. Standley, B.; Bao, W.; Zhang, H.; Bruck, J.; Lau, C. N.; Bockrath, M. Graphene-Based Atomic-Scale Switches. *Nano Lett.* **2008**, *8*, 3345–3349.
13. Son, D. I.; Kim, T. W.; Shim, J. H.; Jung, J. H.; Lee, D. U.; Lee, J. M.; Park, W. I.; Choi, W. K. Flexible Organic Bistable Devices Based on Graphene Embedded in an Insulating Poly(methyl methacrylate) Polymer Layer. *Nano Lett.* **2010**, *10*, 2441–2447.
14. Milaninia, K. M.; Baldo, M. A.; Reina, A.; Kong, J. All Graphene Electromechanical Switch Fabricated by Chemical Vapor Deposition. *Appl. Phys. Lett.* **2009**, *95*, 183105.
15. Kim, S. M.; Song, E. B.; Lee, S.; Seo, S.; Seo, D. H.; Hwang, Y.; Candler, R.; Wang, K. L. Suspended Few-Layer Graphene Beam Electromechanical Switch with Abrupt on-off Characteristics and Minimal Leakage Current. *Appl. Phys. Lett.* **2011**, *99*, 023103.
16. Zheng, Y.; Ni, G.-X.; Toh, C.-T.; Zeng, M.-G.; Chen, S.-T.; Yao, K.; Ozyilmaz, B. Gate-Controlled Nonvolatile Graphene-ferroelectric Memory. *Appl. Phys. Lett.* **2009**, *94*, 163505.
17. Yong-Joo, D.; Gyu-Chul, Y. Nonvolatile Memory Devices Based on Few-Layer Graphene Films. *Nanotechnology* **2010**, *21*, 105204.
18. Song, E. B.; Lian, B.; Kim, S. M.; Lee, S.; Chung, T.-K.; Wang, M.; Zeng, C.; Xu, G.; Wong, K.; Zhou, Y.; *et al*. Robust Bi-Stable Memory Operation in Single-Layer Graphene Ferroelectric Memory. *Appl. Phys. Lett.* **2011**, *99*, 042109.
19. Tsai, W. J.; Zous, N. K.; Liu, C. J.; Liu, C. C.; Chen, C. H.; Tahui, W.; Pan, S.; Chih-Yuan, L.; Gu, S. H. Data Retention Behavior of a SONOS Type Two-Bit Storage Flash Memory Cell. *IEDM Tech. Dig.* **2001**, 719–722.
20. Wang, S.; Pu, J.; Chan, D. S. H.; Cho, B. J.; Loh, K. P. Wide Memory Window in Graphene Oxide Charge Storage Nodes. *Appl. Phys. Lett.* **2010**, *96*, 143109.
21. Malard, L. M.; Pimenta, M. A.; Dresselhaus, G.; Dresselhaus, M. S. Raman Spectroscopy in Graphene. *Phys. Rep.* **2009**, *473*, 51–87.
22. Kim, S.; Nah, J.; Jo, I.; Shahrjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S. K. Realization of a High Mobility Dual-Gated Graphene Field-Effect Transistor with Al_2O_3 Dielectric. *Appl. Phys. Lett.* **2009**, *94*, 062107.
23. Guinea, F. Charge Distribution and Screening in Layered Graphene Systems. *Phys. Rev. B* **2007**, *75*, 235433.
24. Sui, Y.; Appenzeller, J. Screening and Interlayer Coupling in Multilayer Graphene Field-Effect Transistors. *Nano Lett.* **2009**, *9*, 2973–2977.
25. Lee, N. J.; Yoo, J. W.; Choi, Y. J.; Kang, C. J.; Jeon, D. Y.; Kim, D. C.; Seo, S.; Chung, H. J. The Interlayer Screening Effect of Graphene Sheets Investigated by Kelvin Probe Force Microscopy. *Appl. Phys. Lett.* **2009**, *95*, 222107.
26. Wang, H.; Wu, Y.; Cong, C.; Shang, J.; Yu, T. Hysteresis of Electronic Transport in Graphene Transistors. *ACS Nano* **2010**, *4*, 7221–7228.
27. Hong, A. J.; Liu, C.-C.; Wang, Y.; Kim, J.; Xiu, F.; Ji, S.; Zou, J.; Nealey, P. F.; Wang, K. L. Metal Nanodot Memory by Self-Assembled Block Copolymer Lift-Off. *Nano Lett.* **2009**, *10*, 224–229.
28. Romero, H. E.; Shen, N.; Joshi, P.; Gutierrez, H. R.; Tadigadapa, S. A.; Sofo, J. O.; Eklund, P. C. n-Type Behavior of Graphene Supported on Si/SiO_2 Substrates. *ACS Nano* **2008**, *2*, 2037–2044.
29. Liu, L.; Ryu, S.; Tomasik, M. R.; Stolyarova, E.; Jung, N.; Hybertsen, M. S.; Steigerwald, M. L.; Brus, L. E.; Flynn, G. W. Graphene Oxidation: Thickness-Dependent Etching and Strong Chemical Doping. *Nano Lett.* **2008**, *8*, 1965–1970.
30. Chen, J.-H.; Jang, C.; Xiao, S.; Ishigami, M.; Fuhrer, M. S. Intrinsic and Extrinsic Performance Limits of Graphene Devices on SiO_2. *Nat. Nano* **2008**, *3*, 206–209.
31. Li, X.; Cai, W.; Colombo, L.; Ruoff, R. S. Evolution of Graphene Growth on Ni and Cu by Carbon Isotope Labeling. *Nano Lett.* **2009**, *9*, 4268–4272.
32. Yu, Y.-J.; Zhao, Y.; Ryu, S.; Brus, L. E.; Kim, K. S.; Kim, P. Tuning the Graphene Work Function by Electric Field Effect. *Nano Lett.* **2009**, *9*, 3430–3434.
33. Guan, W.; Long, S.; Liu, M.; Liu, Q.; Hu, Y.; Li, Z.; Jia, R. Modeling of Retention Characteristics for Metal and Semiconductor Nanocrystal Memories. *Solid-State Electron.* **2007**, *51*, 806–811.
34. Ki-Tae, P.; Myounggon, K.; Doogon, K.; Soon-Wook, H.; Byung Yong, C.; Yeong-Taek, L.; Changhyun, K.; Kinam, K. A Zeroing Cell-to-Cell Interference Page Architecture With Temporary LSB Storing and Parallel MSB Program Scheme for MLC NAND Flash Memories. *IEEE J. Solid-State Circuits* **2008**, *43*, 919–928.
35. Rasool, H. I.; Song, E. B.; Allen, M. J.; Wassei, J. K.; Kaner, R. B.; Wang, K. L.; Weiller, B. H.; Gimzewski, J. K. Continuity of Graphene on Polycrystalline Copper. *Nano Lett.* **2010**, *11*, 251–256.
36. Rasool, H. I.; Song, E. B.; Mecklenburg, M.; Regan, B. C.; Wang, K. L.; Weiller, B. H.; Gimzewski, J. K. Atomic-Scale Characterization of Graphene Grown on Copper (100) Single Crystals. *J. Am. Chem. Soc.* **2011**, *133*, 12536−12543.